REMARKS/ARGUMENTS

In this amendment, claims 1-17 are cancelled, and claims 18-27 are added. Support of new claims 18-27 can be found in original claims, Figure 4 and its relevant descriptions.

35 USC 112 rejection: Since claims 1-17 have been cancelled, no 35 USC 112 issue exists any longer.

35 USC 102 and 103 rejections: None of the cited references and their combinations discloses or suggests the subject matter as recited in claim 18. According to prior art, when there's need to fix functional or timing issues, logic designers have to analyze the problems, modify the netlist, then handoff the second netlist to physical designers for physical design change (known as timing ECO or functional ECO; ECO: Engineering Change Order). A netlist has to be transferred back and forth between the logic designers and the physical designers until all the errors of the netlist have been corrected. On the other hand, according to the present invention, the database can be automatically updated while automatically updating other kinds of description instructions. The logic designers can predict the effect of the change right after the modification, and see possible issues (could be timing, power, or noise issues) before the physical design change is really implemented, so that the number of the iterations between the logic designers and physical designers will be reduced. For example, as described on page 8, second paragraph, of the present specification, the first interface 22 is capable of updating any information of the core database, which is in equivalent corresponding to the ASIC 50, the logic unit 24 is capable of updating the remaining information of the core database according to the updated information, and the display panel 26 is capable of displaying the noise analysis report on the noise analysis report window 32, the netlist on the netlist window 34, the layout of the ASIC 50 on the physical circuit window 36, and the timing

slack report corresponding to the netlist of the ASIC 50 on the timing slack report window 38 in accordance with the display instructions input to the keyboard 22 or the mouse 22. The logic designers therefore are able to update the circuit component information shown on any one of the windows 32, 34, 36 and 38, without the need to ask for the help offered by the physical designers.

In view of the foregoing, the new claims are patentable over the cited references.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)